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SCULLY SCOTT MURPHY & PRESSER, PC
400 GARDEN CITY PLAZA
SUITE 300
GARDEN CITY, NY 11530

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PADGETT, MARIANNE L	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/674,648	CHOE ET AL.	
	Examiner	Art Unit	
	Marianne L. Padgett	1762	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Use of relative terms that lack clear metes and bounds in the claims, or in a clear definition provided in the specification or cited relevant prior art, is vague and indefinite. The term "graded" may be considered a relative term, or at least ambiguous, as its meaning varies depending on its context. As presently employed in all the independent claims 1, 37 & 38 to describe "a graded porous Si-containing structure" or "... region" that may have a multiplicity of possible meanings, such as graded in quality, or graded in shape, as in a sloping surface, or graded in composition, as in a gradient of a component or element, or graded microstructure, such as a gradient in degree of porosity, etc. As presently written, the claims could be considered broadly inclusive of all such possibilities, or vague and indefinite, because it is ambiguous or uncertain what meaning is intended for the modifier gradient as applied to the porous Si-containing structure or region. The examiner notes that the specification, as seen in the abstract's recitation of "The graded porous Si has a relatively coarse top layer and a fine porous layer that is buried beneath the top layer", provides EXAMPLES of applicants' intent, however examples do **not** constitute a definition, and the claims as written are directed to considerably broader scope than such specific examples, therefore it appears that in order for applicants' intent to be clear in the claims, the intent needs to be explicitly recited in the claims.

The action of "activating", as recited in claim 2 for "activating the dopant", may be considered a relative term, since the dopant is a generic implanted ion, where the purpose of the doping is unspecified, such that what constitutes activating an unknown dopant for an unknown purpose cannot clearly be determined. It is noted that claim 3, which specifies n-type or p-type dopants overcomes this problem by using art recognize descriptions of particular categories of semiconductor dopants, where activating

would presumably require that the activating enables the n-type or p-type doped regions to act as electron accepting or a hole creating regions.

The modifier "neutral" used to describe "neutral ion" in claims 31-34, is also a relative term, and while a definition is found in paragraph [0040] that states that the neutral ions do not interact with the Si-containing substrate (see section 2 below), that definition contradicts teachings in the same paragraph, as well as requirements in claims, such as 33 where the neutral ions interact by making a region amorphous, thus does not provide a usable or unclear definition for what the term "neutral ion) encompasses. Claims 32 & 34, which define the specific "neutral ion" that is used, overcome this problem with respect to what the neutral ion is, but **not** as to what it does.

The examiner also notes that the modifier "uniform" used in the claims to describe "a uniform buried oxide layer" is defined in paragraph [0024], which states "The term 'uniform' is used in the present invention to denote a buried oxide layer having a continuous interface with the Si-containing over layer as well as the underlying Si-containing substrate wherein the variation of thickness across the entire wafer is less than 20% of the total buried oxide thickness", thus defining "uniform" to have this meaning no matter what it is describing in this application. (Did applicants actually mean to only give "uniform" this definition **when** it was associated with a buried oxide layer?) It is further noted that this definition causes some uncertainty with respect to the claims 1 & 38, because it requires that there be a "Si-containing substrate" underlying the "uniform buried oxide layer", but neither of these claims necessarily provide any "Si-containing substrate" when they provide the claimed "graded porous Si-containing structure", which only needs to have some portion or part therein be Si-containing, that could easily be a surface layer, not substrate. Therefore, it is uncertain where or if the requirements of the definition for "uniform" were supplied in the claimed process, making it uncertain as to whether or not they were even intended to be claimed, despite the definition in the specification.

The examiner notes that "inert gas" is generally not considered a relative term, because it has an art recognized meaning, i.e. is the same thing as a noble gas or a rare gas, in other words the last column of elements in the periodic table, however in applicants' specification in [0043-45], there are given "examples" of inert gas atmospheres and/or oxidizing ambients as "He, Ar, O_2, N_2 and mixtures thereof". As this is not a definition, it is not binding on the claim language, but this discussion in the specification does shed doubt on the meaning in the claims, especially considering that with respect to silicon, nitrogen is reactive, thus fitting neither relative meaning nor periodic table meaning of "inert gas".

In claims 14-15 & 23-24, dependent from independent claim 1, "the porous Si-containing **region**" lacks proper antecedent basis due to inconsistent terminology, as no regions have been introduced in the independent claim, whose limitations are directed to "a graded porous Si-containing **structure**" (emphasis added).

Similarly in claims 16-17, dependent from claim 1, which is forming a further layer "atop the Si-containing **substrate**" (emphasis added) lacks proper antecedents and clear instructions due to inconsistent terminology, since there was no substrate introduced in the body independent claim. It is noted that the word "substrate" is used as a modifier in the preamble in the phrase "a silicon-on-insulator substrate structure", but the "substrate" used therein is not connected to the body of the claim, nor does it require that whatever entity one calls a substrate in the structure is silicon-containing. A clear or positive connection between any claim of "Si-containing substrate" & preceding claim limitations/claims is especially important, as applicant specification requires that "The term 'Si-containing substrate' as used herein the notes a semiconductor material that includes at least silicon" ([0035]), hence requiring a narrower scope of materials than its literal meaning, and where the broader limitation of "... Si-containing structure" has no such narrowing of scope, hence need supply no semiconductor materials to the process, such that any structure that's porous, is in some way graded & contains at least silicon (i.e. silicides; or silicon oxides, nitrides, carbides, etc.) are encompassed.

Results of the oxidizing step as further defined by claim 22 is somewhat confusing, in that it is unclear if claim 22 is contradicting the requirement of the independent claim 1, which appears to have the oxidizing step forming the "uniform buried oxide layer", or that this claim means that the buried layer was part of the initial structure (i.e. is not formed by the process) & it is the surface oxide that is being formed, or if the process is intended to be forming both oxide layers at once (i.e. oxidizing the surface at the same time as forming a buried oxide layer). This claim could be said to shed doubt on the meaning of "oxidizing" in the independent claim.

In claim 24, dependent from claim 1, "said buried oxide" as inconsistent terminology with respect to the previously introduced term "a uniform buried oxide **layer**" (emphasis added), however as it is the only previously introduced term to which the article "said" that indicates antecedent basis could be referring, it would be reasonable to assume that "said buried oxide" must refer to "uniform buried oxide layer", except that by definition in the specification, continuous interfaces between over and under layers are required to exist which in turn requires the buried layer to be continuous, thus is contradicted by the requirement of claim 24 of "comprises discrete islands of thermal oxide".

The meaning of claim 25 is completely unclear. When and how are the discrete islands of both the "porous Si and buried oxide" consumed? Consumed by what or for what purpose or to produce what? Is the purpose of this dependent claim to destroy what was made in the independent claim, since one is "consuming" the buried oxide which is required to be in the SOI structure that is being fabricated; is that what consumed means? The claim is further unclear considering that there is no actual claim anywhere of the necessary existence of "porous Si", only of "porous Si-containing region" or "graded porous Si-containing structure" or "silicon-containing over layer", or considering the definition of "uniform", the Si-containing substrate, which is actually a Si-containing semiconductor substrate.

The meaning of claim 26 is unclear, as it is uncertain how providing multiple graded porous Si-containing structures & separately oxidizing these structures provides **a single** "multi-layered Si-on-

insulator material". It is noted that if as according to the definition of "uniform", the produced structure must have at least a Si-containing over-layer/(uniform) buried oxide layer/Si-containing substrate, then each resultant structure has at least three layers, hence each is "multilayered".

The phrasing in claim 34 is a bit awkward, since as written the concluding phrase "at or below nominal room temperature" appears to be associated with "and an implant energy...500 keV", but the examiner assumes due to logic and typical process procedures that the intent is that --said implanting step is performed at or below nominal room temperature using...--.

With respect to claim 35, the examiner notes that the "uniform buried oxide layer", which limitation is in the independent claim from which claim 35 depends, by definition ([0024]) requires the buried oxide layer to be continuous, in order for it to have a continuous interface with the overlying Si-containing layer & underlying Si-containing substrate. Hence, while by definition the required "a broken buried oxide region" **can not** be part of the "uniform buried oxide layer", it is uncertain whether or not "a continuous buried oxide region" is part of the "uniform buried oxide layer" or separate therefrom. It is further unclear to the examiner how this one oxidizing step creates two or three different buried oxide layers &/or regions, and exactly what is their relationship in the process.

2. The disclosure is objected to because of the following informalities: paragraph [0040] has contradictory teachings, as first it teaches that "a neutral ion that **causes damage** formation within the Si-containing substrate 10 is used...", but then it defines the "term 'neutral ions' is used in the present invention to denote any ion that does not **interact** with the Si-containing substrate 10" (emphasis added), however causing damage is a very definite and explicit form of interaction with the silicon-containing substrate, hence these 2 subsequent sentences directly contradict each other. Note that the verb "interact" is a broad term that covers any kind of affect that the "neutral ions" may have on the Si-containing substrate, inclusive of etching, sputtering, chemical reactions, creation of dangling bonds or other disruption of bonds, ionization, heating, momentum transfer, etc., and for there to be no interaction

between the two, any "neutral ion" as defined must pass through the substrate without having any effect whatsoever upon the substrate. Note that some subatomic particles, such as neutrinos (which are not ions), are known for not interact with matter except upon rare or infrequent occasions & circumstances, but ions in planting into a substrate can rarely be accurately said to have no interaction therewith.

In paragraph [0048], it states that "find porous region 16a is located mostly at the bottom of the porous region 16, while courser porous region 16b is located mostly at the top of porous region 16", however as illustrated in figures 1C & 1D, 16a is on the top, while 16b is on the bottom, hence unless this figure is upside down, the body of the specification is contradicting the figure. Also note that with respect to "fine" and "courser", a hand-drawn schematic without specified scale or key cannot be used to support a specific relative density configurational relationship.

Appropriate correction is required.

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1, 12-14, 16-18, 21, 23-24 (25), 26, 35 & 38 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Ikeda Tadashi (JP 09-064323; also see Patent Abstracts of Japan & 2 machine translations).

Ikeda teaches employing a semiconductor substrate, that may be a silicon wafer, which has been doped to be either n-type or p-type, and treating it with a HF solution, with an exemplary current density of 10-80 mA/cm^2 creating a porous silicon layer of a desired thickness (~ 100 nm exemplified) via anodization (figures 1 (a-b) & 2 (a-b); [0015-16]; [0022] & [0027]). Note a silicon substrate, with part thereof turned to a porous layer, has part porous & part not porous, hence may be considered graded with respect to the porosity. Thereafter, a single crystal silicon layer is deposited over the porous silicon layer, then oxygen ions are implanted through the single crystal silicon layer into the porous silicon layer as part of the oxidation process (an O-containing ambient is clearly present), after which heat treatment is performed at temperatures of 1200-1350°C, so as to form an "embedded oxide film layer" from the ion implanted porous layer, which due to the overall oxidation processing technique is taught to not increase in volume from that of the original porous layer. Options of uniformly ion implanting the substrate, or using a patterned resist to mask areas during ion implanting, with potentially multiple ion implantings are taught (figures 1 (c-e) & 2 (c-e); [0017-19] & [0022-25]). Ikeda notes that their techniques solve

problems discussed with respect to the conventional processes illustrated in figures 3 & 4. With respect to uniformity of buried oxide layer, if one considers the relative meaning of the term, it may be considered covered by Ikeda. If the definition in applicants' specification (which contradicts the patterning claims, etc., see above 112's) is considered, the required three layers are present, and while no discussion in Ikeda requires the variation in the buried layers thickness to be less than 20 % of the total buried layer thickness, Ikeda's technique is trying to solve problems of stress & volume expansion beyond the porous layer, so as to not cause **unevenness** of the buried layer ([0010], [0019] & [0025]), such that for continuous buried layers a uniformity within 20% would appear to be encompassed, or alternately it would have been obvious to one of ordinary skill in the art to control processing and as taught so as to prevent unevenness to such a degree as defined, due to the suggestion that unevenness is a problem to be solved. For claimed patterned buried layers, uniformity as defined is impossible, hence cannot be discussed in the context of the definition, but would be considered covered in the context of the relative term. (Claim 25 might be considered to be included in this rejection, if it is considered that formation of the buried oxide layer consumes the porous area, but it does not appear to be possible to make any SOI having a buried oxide layer as claimed, if one is required to "consume" the buried oxide, such that the required insulator is no longer present.)

While Ikeda teaches creating a porous layer (≡ porous Si-containing region), the percentage of that layer which is porous is not disclosed, however at the claimed range of "about 0.01 % or greater" is so broad that it covers virtually any conceivable amount that may be produced by Ikeda's process & still be called porous. Furthermore, the anodization technique used by Ikeda to create the porosity is essentially the same as the anodization process claimed by applicants & discussed in applicants' specification on [0049-53] as used to convert doped single crystal silicon to porous silicon, thus like porosities would have been expected to have inherently been produced from like processes & materials. Alternately, it would've been obvious to one of ordinary skill in the art to create sufficient porosity in

order to effect Ikeda's taught process of creating an embedded or buried oxide layer, where volume increase is not a problem (i.e. avoid crystal & stress defects caused by increased volume during oxidation), such that the compositional parameters, such as degree of doping & the HF anodization parameters would have been optimized based on those taught in order to produce required porosity for required effects.

5. Claims 2-11, 15, 19-20, 22 & 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda Tadashi, optionally considering Hiromitsu Namita (JP 62-245620, translation ordered, not yet received) or Hidekane Ogata (JP 2-164023, translation ordered, not yet received).

While Ikeda discussed treating a doped (n-type or p-type) silicon substrate, they do not teach particular dopants, the means for effecting the doping, nor require activating the doped region, however it would've been obvious to one of ordinary skill in the art to employ standard n- or p-type dopants & conventional means for silicon wafer doping, which would have been expected to be inclusive of p-type dopants, such as B, it source gases, such as boron fluoride, & conventional means for implanting dopants, such as ion implantation, where ion implantation would have been expect to be especially considered as Ikeda's process is already employing ion implantation techniques, thus equipment therefore would already have been available, providing an economic incentive for employing known ion implanting techniques. Particular ion energies & doses would have been determined by routine experimentation, plus knowledge of the old and well-known process of creating porosity via electrolytic anodization, where required depth, thickness & degree or porosity would have been used in determination of suitable dose and energy. As the need to activate ion implanted dopants is old, well known & would have been known to be necessary in order for the dopants to do their required job with respect to the anodization, activating would have been a recognized required step to one of ordinary skill & competence in the art, who would've employed any known & conventional annealing technique and parameters therefore that would have been expected to the effective on the particular semiconductor substrates being employed. Note that

as ion implantation to form a layer will inherently cause a gradation of dopant concentrations, due to cross-section effects of ion stopping power for particular energies & materials, thus causing a gradient in the electrical potential with respect to the graded dopant concentration, so the electrolytic anodization process when applied to ion implanted dopant in silicon would have inherently produced a gradation in degree of porosity that varies with respect to the dopant concentration.

Alternately, the Japanese references to Namita or Ogata both teach p-type ion implantation into silicon as preparation for creating porous silicon via electrolytic anodization, thus substantiating the above asserted obviousness, where Namita's English abstract is generic with respect to the p-type dopant, but specifically illustrates annealing the ion implanted doped silicon before performing the anodic process in hydrofluoric acid, while Ogata's English abstract explicitly demonstrates the expected usefulness of ion implanted B for creating a porous structure using floric acid electrolytic solution in the anodic formation process. Thus either of these optional secondary references provide evidence of the known and expected usefulness of ion implantation for creating the require doped regions for electrolytic anodic creation of porous silicon for use in SOI structure formation, further showing the above stated obviousness. Also note, that if applicants' claim 31 did not have an impossible definition applied to "neutral ion", the implantation of a proton (H^+) after ion implantation of the p-type dopant in Namita, might be considered to read on claim 31, as the implantation of hydrogen into the silicon substrate might be considered equivalently interactive as the implantation of Si into the silicon substrate, an element that applicants exemplify as useful as a "neutral ion", but at present it is impossible to define what "neutral ion" might encompass besides the specifically designated elements.

While Ikeda teaches the heat treatment at temperatures of 1200-1350°C encompassed by the claims relevant to claimed oxidizing or "post oxidation step" temperatures, Ikeda does not discuss the atmosphere under which this heat treatment to create the embedded oxide layer is performed, however it would've been obvious to one of ordinary skill in the art to employ atmospheres which either further the

oxidation process, prevent contamination during oxidation or the like, such than that as an oxide is being created, it would have been obvious to employ atmospheres that have an oxygen ambient using a common source of oxygen, such as those claimed, where the atmosphere is otherwise unreactive (which obvious logic would suggest to one of ordinary skill in the art use of inert gases to achieve desired pressure, prevent contamination, or like standard purposes), since such would have been expected to prevent out-gassing of oxygen, which would decrease the desired stoichiometry, & since performing oxidations under oxygen atmospheres is a standard procedure. It is noted that use of such an oxygen containing atmosphere during the heat treatment process/annealing would inherently affect the surface of the single crystal silicon layer to affect thermal oxidation thereon, and as such would be further desirable for particular device formation sequences which require such a surface oxide layer. Alternately, the use of the hydrogen ambient would've prevented undesirable reactions with the silicon surface & performing surface passivation thereof, a known desirable effect for many semiconductor device layers.

6. The background in deSousa et al. (5,188,978; col. 1, line 16-31) is cited for its clear showing that it is old and well-known in the semiconductor art that it is necessary to anneal the semiconductor after ion implantation in order to remove damage caused thereby, so as to appropriately affect or optimize electrical properties and carrier mobility.

7. Claims 1-26, 29-30, 35-36 & 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Houston et al. (2002/0086463 A1), optionally considering Hiromitsu Namita (JP 62-245620, translation ordered, not yet received) or Hidekane Ogata (JP 2-164023, translation ordered, not yet received) for claims 2-11.

Houston et al. teach making an silicon-on-insulator (SOI) wafer, where a first layer of porous silicon is formed by anodizing a boron (i.e., p-type) doped silicon wafer using a HF solution, such that the depth of the porous silicon is controlled by the timing of the anodization treatment or by limiting the depth of the boron doping, where thicknesses in the range of nanometers to microns can be obtained

([0006]; [0016]). Note, one of ordinary skill would find this a clear suggestion that if presence of dopant is a determinant in the depth of porous microstructure formed, then concentration of that dopant would also be a factor in the amount of porosity formed. Houston et al. teach that the anodizing process can result in cracks on the surface of the porous silicon, hence they employ a "prebake" process that fills up surface pores with migrated silicon atoms in order to reduce the surface energy. This "prebake" process seals the surface; may employ a hydrogen ambient; and it may provide a starting point for subsequent epitaxial growth of a layer on the surface, where the quality of the epitaxial layer may depend on the surface pore filling during the sealing bake ([0006]; [0018-19]; [0022]). The epitaxial semiconductor layer may be deposited on the sealed surface either before or after oxygen ion implanting, where the ion implanting may be carried out via plasma oxygen implant or other oxygen implanting methods, with the oxidizing species derived from molecular oxygen or other sources, such as ozone or N_2O, and where oxygen doses may be on the order of 10^{17}-10^{18} oxygen ions/cm^2 ([0006]; [0016]; [0020]; 0023-25] & [0031]). The oxidation process, which forms the buried oxide layer from the implanted oxygen is completed by "high-temperature anneal", which appears to use temperatures on the order of 1000°C for about 30 minutes ([0006] & [0020]), but does not specify the atmosphere employed during the anneal, however choices of atmospheres, such as oxygen containing, inert gas containing, H-containing, would have been obvious for reasons as discussed above in section 5, as the process of Houston et al during the post oxygen implantation annealing would have been analogous to those discussed above, especially considering discussion in Houston et al. concerning various oxygen gas sources, as well as H-annealing processing in preceding steps. Houston et al. teach their process provides a number of advantages ([0007-11]), inclusive of aiding a planarity, sharp definition of the oxide layer, etc.

The teachings of Houston et al. differ from the present claims by not discuss as uniform, the buried oxide layer made from the porous layer, its oxygen implantation & anneal thereof, however as Houston et al. teach means for controlling the thickness of the porous layer, hence the buried oxide layer,

suggesting its thickness measurements can be in the range of nanometers which would be suggestive of a degree of uniformity consistent with that in applicants' specification's definition, and Houston et al.'s layer sequence is consistent with applicants' definition, as it must be applied to the claims if it is employed at all. It would have been obvious to one of ordinary skill in the art that the taught control of depth of the porous layer & contemplated thicknesses for the buried oxide is suggestive of care being taken to create even layers, such that a uniformity of thickness of less than 20% of the layer's thickness would have been well within expected uniformity & reproducibility, especially as the intended use relates to integrated circuit structures where miniaturization, reproducibility, does uniformity can be crucial, and Houston et al. teach advantages of planarity & sharp definition, which are also suggested & supported of uniformity as defined for variation by applicants.

While Houston et al. discusses boron doping to control depths, they do not specify the depth doping performed by ion doping, however such techniques, including activation/annealing of the doped silicon containing substrates, thereafter would have been obvious for reasons as discussed above in section 5, optionally considering secondary references to Hiromitsu Namita (JP 62-245620,) or Hidekane Ogata (JP 2-164023) for reasons also discussed in section 5 above.

Houston et al. did not provide claimed parameters for current densities for the anodization process nor for the ion implantation process, nor ion beam energies for implantation, nor temperatures for baking/annealing to seal the porous surface in the hydrogen ambient, however given the taught process & objectives of Houston et al., one of ordinary skill in the art would have been expected to employ routine experimentation to determine necessary parameters not explicitly given, such as current densities, energies & temperatures, in order to employ the taught procedure to produce the taught results, which would have been expected to be inclusive of claimed ranges, as no critical differences seen in their effects. Note that Houston et al.'s teaching of the implanting oxygen with plasma or other ion implantation methods, would have been suggestive to one of ordinary skill in the art of oxygen plasmas or

oxygen ion beams to effect the oxygen implantation, where the parameters of either technique would have been optimized to produce doses on the order claim, noting that in paragraph [0006] Houston et al. teach implantation of low oxygen doses, and that the 10^{18} O ions/cm^2 is considered to be a relatively heavy dose [0020], which teachings would suggest to one of ordinary skill an apparent preference for the lower end of the taught dosage range.

It is noted that while Houston et al. has much discussion on growing of an epitaxial layer (epi layer), its material is generally not identified, although [0023 & 25] refers to it as an epitaxial semiconductor layer, but [0024] in analogous sequence only refers to a semiconductor layer, not mentioning epitaxial, while [0006] also does not discuss an epitaxial layer in the process sequence, instead discusses forming a thin silicon film by standard deposition techniques on the sealed porous silicon layer, hence growth of an epitaxial silicon layer on the sealed H-prebaked surface is considered taught or suggested by Houston et al., or alternatively obvious due to the overlapping of the teachings for the desired deposit on the sealed surface as presented above.

8. Claims 1-26 & 29-38 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-25 of copending Application No. 10/674,647. Although the conflicting claims are not identical, they are not patentably distinct from each other because the two applications contain process limitations directed to the same or analogous steps with overlapping ranges, claimed in different orders to produce variations in scope, and employing varied nomenclature to effect semantics or scope differences. For instance, the present case starts with "providing a graded porous Si-containing structure", while the (647) application is providing "a structure comprising at least a Si-containing substrate that has a region of vacancies or voids located therein", where it is noted that voids can be considered equivalently to porosity & in both these cases n-type or p-type dopants are employed & like electrolytic anodization process in the "providing..." steps, which according to applicants' specification ([0047-53]) is what produces the graded porous microstructure

within the Si-containing substrate /structure, hence these limitations, when considered with their dependent claims further defining the providing steps, are seen to be equivalent and/or significantly overlapping. Similarly, the dependent claims concerning forming a capping layer are overlapping with the (647) application's dependent claims of forming a [single crystal] silicon-containing layer (112 problems). The various annealing, "pre-oxidation", "post oxidation", ion implanting & oxidizing steps in the dependent claims of the present application are of overlapping scope with the bake step, implanting step, annealing of the copending application (647). Thus, the claims of these two applications may be considered obvious variations on a theme with highly overlapping scope. It is noted that the present application has limitations to specific annealing techniques of furnace anneal, rapid thermal anneal or spike anneal, whereas the copending (647) case is generic as to the type of bake or anneal technique, however temperatures & gases employed, as well as materials overlap, with analogous uses, hence it would've been obvious to one of ordinary skill in the art to employ any of the specifically named conventional heating/annealing techniques for the generically claimed baking/annealing of copending (647), where particular parameters would have been expected to be determined & optimize the routine experimentation dependent on the particular silicon-containing materials employed, as well as desired depths & thicknesses of buried oxide layers being produced.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

9. Claims 1, 12, 14 16-24 (25), 26, 31-36 & 38 are rejected under 35 U.S.C. 102(e) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Bendernagel et al. (6,800,518 B2, which incorporates PN 5,930,643 to Sadana et al. by reference).

Claims 2-11, 13 & 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bendernagel et al., in view of Hiromitsu Namita (JP 62-245620, translation ordered, not yet received) or Hidekane Ogata (JP 2-164023, translation ordered, not yet received) as discussed above

The applied reference has a common assignee & overlapping, but not identical inventors with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Bendernagel et al. teach forming composite structures, which may include buried insulators (oxides), buried conductive & buried void plane structures, by forming a layer of porous silicon (or alternately forming vacancies or voids) in the surface region of a semiconductor substrate, such as silicon via electrolytic anodization with a HF-containing solution, where the porosity produced is mainly dependent on the current (~0.1-20 mA/cm^2) & voltage (~0.1-10 volts typical, ~0.5-5 volts preferred) used, the HF concentration, and the **dopant type & concentration** in the wafer, and where thickness of the porous silicon layer may additionally depend on the time (~30 sec.-10 min.,~1-5 min. more highly preferred) of anodization process. For this process, Bendernagel et al. teach that the "semiconductor **wafer needs to be doped**, preferably but not necessarily with **p-type** doping atoms. When a **boron**-doped p-type wafer is employed, the dopant concentration of the wafer is typically from about 1E15 to about 1E19 $atom/cm^3$..." (emphasis added, col. 6, lines 18-26). Next it is taught that a brief anneal in hydrogen ambient at elevated temperatures may be employed to eliminate open pores on the surface of the porous silicon layer, thereafter an epitaxial silicon (epi-Si) layer on the surface, then the composite substrate is ion implanted, where the ions employed may be oxygen ions, when a buried oxide is intended, or optionally may include nitrogen ions, or just use nitrogen ions for an alternate buried insulator, or metal ions for a buried conductor or void planes. Masking may optionally be employed, with a HF-resistant material (photoresist) before the anodization step &/or a patterned mask for selective ion implantation before implanting, which masks are removed before deposition of the epi-Si or after ion

implanting, respectively. Oxygen ion implanting may be in a single or multiple steps, continuous or pulsed, or combined with other ion implantation steps depending on desired structure. Oxygen implanting is taught to be via any conventional ion implantation apparatus, with any conventional ion implanting conditions employed, which are exemplified as O-ion dose from about 1E16-2E18 atoms/cm^2, implantation energy from about 50 KeV-10 MeV, ion beam current density from about 0.05-500mA/cm^2, and ion implantation temperature from about 480-650°C. More preferred oxygen ion implantation conditions are also given (~5E16-2E17 atoms/cm^2, ~150-300 KeV, ~1.0-10 mA/cm2, ~550-600°C) as well as the high-temperature ion implantation step, followed by a normal room temperature ion implantation step exemplified in prior art references. After the ion implanting step(s), high-temperature annealing is performed to transform the implanted oxygen regions into buried oxide regions, while regions that do not contain oxygen ions can be transformed into void layers or buried conductive regions. The high-temperature annealing in is performed at temperatures of about 1300°C or greater, but less than the melting point of Si , which is 1415°C, and may be carried out in atmospheres of pure oxygen (O_2), oxygen mixed with an inert gas or N_2, or either without oxygen, or vacuum. When annealing causes significant diffusion of dopants into the overlying silicon layer, a "post" hydrogen annealing process, which may use the same or different conditions (0.25-3 hours, $\leq$ 82 Torr H-ambient, T = 1100-1150°C), is then employed. Col. 9, lines 7-12 notes that during annealing, the porous silicon is **consumed** by the formation of the buried oxide/void, and that the epi-Si layer may be thinned by surface oxidation.

Bendernagel et al. teach that the thickness of various layers of the composite structure may vary depending on process conditions employed during fabrication, where typically the buried insulating region has a more highly preferred thickness from about 5-200 nm, and that the thickness of the buried insulating regions is dependent on device requirement and could be **controlled** by adjusting vertical depth of the porous silicon layer form during HF-anodization and the dose of the implanted ions. They are also teaching the possibility of multiple implantations to form different layer structures or side-by-side

structures, thus suggesting a reasonable degree of reproducibility or controllability of layer thickness, which would also suggest to one of ordinary skill a similar degree of uniformity where desired, thus for the relative meaning of "uniform", Bendernagel et al. is considered to encompass the claimed "uniform buried oxide layer", or alternately considering the definition of applicants' specification, all the requisite layers are present and given the suggested reproducibility or controllability of the thickness taught for the process, it would've been obvious to one of ordinary skill in the art to control the formation of the buried oxide layer to the degree of providing uniformity as defined, in order to provide layers useful for the types of SOI structures & devices intended to be formed. In the specification of Bendernagel et al., particularly see the abstract; col. 2, lines 58-68; col. 3, lines 20-30 & 40-col. 4, line 44; col. 5, lines 10-15 & 27-39; col. 6, lines 17-col. 10, line 40, especially col. 6, lines 17-col. 7, lines 8 for doping & anodization, col. 7, lines 9-31 for H-anneal to eliminate open surface pores, col. 7, lines 32-44 for the epi-Si layer, typically monocrystalline structure ≡ single crystal, col. 7, lines 45-67 for masking, col. 8 for ion implanting & col. 9 for annealing.

While Bendernagel et al. have extensive discussion of doping, including control of dosage & depth thereof, they do not actually specify ion implantation to effect the doping, however such ion implantation would have been obvious for reasons as discussed above (section 5), especially in view of the secondary references which provide specific means via ion implantation of providing dopants for analogous processing.

With respect to applicants' claims 31-34, which is directed to "neutral ion" implantation step, Bendernagel et al's teachings on col. 8, lines 25-54 might be said to overlap with these implantation steps as they are directed to implantation of atoms besides oxygen & after the doping processing. Specifically, beside suggesting multiple ion implantation steps, implantation of elements, such as nitrogen or metal ions inclusive of Mo, Ta, W, or other refractory metals which have eutectic temperature higher than 1300°C, thus implying that no chemical reaction is occurring, might be consistent with applicants'

possible intent of "neutral ions". Furthermore, Bendernagel et al. also suggest looking to other art for ion implantation conditions , such as USPN 5,930,643 by Sadana et al., which was **incorporated-by-reference**, that teaches forming buried oxide layers by creating a damaged buried region in a semiconductor substrate (Si) via ion implantation (O, N, C, Ge, **Bi**, Sb, P, & As), optionally through a capping layer, using a low-dose ion implantation (~≥5E16) at high temperatures about ≥ 200°C, plus a **second** yet lower ion dose implantation to form an **amorphous** layer at same or different energies & same or different ions carried out at cryogenic temperatures to about 300°C, at doses of about 2E14-4E15 ion/cm^2. The ion implantation in Sadana et al. is followed by an oxidation step typically carried out in an inert ambient (N_2 or Ar) mixed with oxygen at temperatures from about 1300°C or higher, with optional further annealing of the oxidized structure (col. 2, lines 10-43), with col. 7 providing three exemplary sequential treatments, including multiple ion implantation that is followed by a sequence of heating steps at various temperatures, such as initially at 200-1000°C in ambient of Ar + 2% oxygen, then at a dozen degrees centigrade in 100% oxygen, followed by 1000-1320°C in ambient of 60% Ar + 40% oxygen, followed by further annealing, were temperature is ramped down, thus providing specific parameters for specific multistep ion implantation alternatives. All the ions in Sadana et al.'s 2 step or multistep ion implantation process have interactions with the silicon substrate, particularly defect formation or **amorphization**, which while contrary to applicants' definition of "neutral ion" is consistent with the required effect of claim 33 of forming an amorphized region. Also, the specifically suggested ion of Bi, is consistent with applicants' claim of that specific ion, hence these incorporated teachings of Sadana et al. (643) are considered to read on applicants' claims 31-33, with the contradictory nature of their specification taken into account. Furthermore, as an alternative suggested ion is Ge, which is chemically homologous with Si, it is considered that

one of ordinary skill in the art would have considered silicon an obvious alternative to this specifically suggested exemplary of ions to be employed in the multi-ion implantation techniques.

10. Claims 1-24 (25), 26, 31-36 & 38 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 14-38 of U.S. Patent No. 6,800,518 B2 (Bendernagel et al.), optionally in view of Sadana et al. (5,930,643).

Although the conflicting claims are not identical, they are not patentably distinct from each other because the Bendernagel et al. claims are directed to the same basic step with overlapping limitations with respect to details, such as parameters, patterning or lack thereof (note that one may selectively implant an area predetermined to be the entire surface, i.e. blanket implantation), order in which specific limitations are emphasized, all of which may be considered obvious variations on the same theme. For instance, the patent to Bendernagel et al. claims forming a porous silicon layer in a surface region using parameters that overlap with claim parameters, thus while the specific porosity ranges or distributions of claims 14 or 15 are not claimed in the patent, due to the almost all-encompassing breath of about 0.1 % or greater porosity in claim 14 & the overlapping electrolytic anodization parameters, the presently claimed porosity range would have been expected to significantly overlap with expected effects of the patented procedure.

With respect to dependent claims 2-3, which require a silicon-containing (i.e. as defined on p.6, [0026] "a semiconductor material that includes at least silicon") substrate, which is doped (n-type or p-type) dopant, the claims in the Bendernagel et al. patent do not mention whether the semiconductor (Si) substrate is doped, however read in light of Bendernagel et al.'s specification, the substrate must be doped in order to perform the claimed electrolytic anodization (col. 6, lines 18-26 & 45-52; col. 7, lines 1-8; & col. 9, lines 41-45), thus n-type or p-type doping is considered to be compassed.

The patent claims also are not directed to uniformity of buried oxide, or layer distribution (, or thickness), however as they are directed to a composite semiconductor structure expected to be used for

finely patterned devices, one of ordinary skill in the art would have expected to produce layer thicknesses typically desirable for such semiconductor devices which would have been expected to have the same degree of uniformity, especially given a lack of significantly different critical procedures, and for that uniformity to be sufficient for taught end uses or devices.

While the patent claims include oxygen ion implantation parameters of dose, implantation energy & ion beam current, as well as repeating the step of oxygen ion implant any number of times which overlaps with presently claimed oxygen ion implantation, including two oxygen implantation steps; the patented claims are not directed to the specific parameter of temperature during single or multiple oxygen ion implantations, however it would have been obvious to one of ordinary skill in the art to employ conventional temperatures for ion beam implantation, which would have been expected to encompass claimed temperature ranges, where choice of temperature would have been expected to be dependent on particular desired structure formation consistent with production of the claimed varied layers, thus expected to encompass claimed temperatures & employ different temperatures when the effects of the two steps are intended to be differentiated, as temperature is old and well known to affect resultant microstructure. Optionally, claimed temperatures for two oxygen ion implantations would have been further obvious in view of Sadana et al. (discussed above in section 9), who is also directed to creating buried oxide regions in semiconductors via oxygen ion implantation, where the desirability of providing two different effects (buried damage region & adjacent amorphous layer) via use of two ion implantations differentiated by dosage & temperature, is taught for controlling resultant oxide thickness & properties (col. 2, lines 1-43+; col. 4, lines 7-29 for first ion implantation & lines 30-65 for second ion implantation; col. 6, lines 8-16 note that the defect containing amorphous region is believed to enhance oxygen diffusion into the silicon & combine with the first created damage layer during the annealing step to form the buried oxide region; figure 2 & col. 6, lines 47-59 this 2-step, 2 temperature ion implantation taught to improve electrical & structural qualities of oxide layer & save implant time & wafer cost), hence it

would've been further obvious to one of ordinary skill in the art given the claimed parameters & claimed multiple ion implantations, to employ a known technique as discussed in Sadana et al. for its taught advantages in producing analogous buried oxide layers using analogous ion implantation with analogous subsequent annealing techniques, with the expectation that advantages taught in Sadana et al. would also be relevant to Bendernagel et al.'s patented process. Also note below discussion concerning obviousness of uniformity in buried oxide regions with respect to Sadana et al.'s .

11. Claims 1, 14, 16-24, 26, 31-33, 35-36 & 38 are rejected under 35 U.S.C. 102(b) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Sadana et al. (5,930,643), which was discussed above in sections 9-10.

As noted above, Sadana et al. (643) has all the parameters to the claimed oxygen ion implanting & annealing steps, for producing buried oxide layers of thicknesses claimed. While Sadana et al. does not discuss providing a silicon-containing semiconductor material in the substrate that has a region with a graded porous silicon symbol-containing structure via the initial ion implanting step, however the initial ion implanting creates defects, with the voids considered to be inclusive of types of defects, thus relevant to the claimed porous limitation, where since such defects or voids are not found through out the entire silicon semiconductor the body, i.e. a layer with voids is formed therein, thus it may be considered "graded", within the possible meaning of the term. Further note that while Sadana et al. most explicitly discuss a 2-step procedure, their teachings are inclusive of "this low temperature/low dose ion implantation step may be carried out in either a single step with a single temperature or multiple steps with multiple temperatures, which range from about cryogenic to about 300°C or less", such that the multistep ion implantation procedure described thereby reads on applicants' plane process, even if one considers the "providing..." step necessarily separate from the step of "implanting...", as the multistep sequence to produce the low temperature low dose implantation, encompasses or overlaps with those sets of applicants' oxygen ion implantation parameters.

Sadana et al. (643) does not describe their buried oxide layer using the adjective "uniform", however as the same process steps as claimed are employ, the resultant effect would have been expected to the of analogous uniformity, whether one considers that term as a relative term, or within the scope of applicants' 20% thickness uniformity, as combined with defined upper & lower layers, which are consistent with those of Sadana et al., or alternately as discussed above it would've been obvious to one of ordinary skill the art to employ the taught process for making SOI structures so as to make sufficiently uniform, reproducible layers useful for semiconductor device formation. Also see preceding obviousness discussions.

12. Sadana et al. (6,222,253 B1) is cited as substantially equivalent to Sadana et al. (643), for purposes of the rejection, except that it only discusses the two-step ion implantation sequences, with analogous subsequent annealing steps, rather than also discussing the option multiple lower temperature & dose oxygen ion implantations subsequent to the initial oxygen ion implantation (summary, especially col. 2, lines 49-col. 3, lines 7; & col. 4, line 10-col. 5, lines 37). However, it is particularly noted that Sadana et al. (253) substantiates the above arguments of including "vacancies" as types of defects created in the initial oxygen ion implantation step, since in col. 4, lines 40-49 oxygen ion implantations in doses of $(3\text{-}5)10^{17}$ ion/cm^2 are explicitly taught to cause "Si damage clusters of Si atoms, Si in interstitial locations and Si vacancies with and/or without oxygen", which can be considered microstructural voids.

Roitman et al. (6204546 B1: abstract; summary; col. 2, lines 44-col. 4, lines 24) has substantially equivalent disclosure to Sadana et al. ((253) or (643)) for purposes of the rejection, except is more similar to (253) & teaches at the first ion implantation creates "silicon crystal and defect regions having stacking faults and dislocation defects" (col. 2, lines 56-57), where dislocation is considered to be substantially equivalent to vacancies, and discusses buried oxide layer thicknesses in the range of 300-800 Angstroms (i.e. 30-80 nm).

13. Claims 1, 14, 16-24, 26, 31-33, 35-36 & 38 are rejected under 35 U.S.C. 102(e) as being anticipated by Norcott et al. (6,486,037 B2, which is the child of PN 5,930,643 to Sadana et al & contains essentially the same teachings with respect to the claims as written).

The applied reference has a common assignee & overlapping, but not identical inventors with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Claims 1, 14, 16-24, 26, 31-33, 35-36 & 38 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-39 of U.S. Patent No. 6,486,037 B2 (Norcott et al.), as discussed above & with respect to its parent Sadana et al. (5,930,643). Although the conflicting claims are not identical, they are not patentably distinct from each other, because the varying semantics, different orders of claiming limitations & overlapping ranges create obvious variations on a theme, where the more specific independent claim limitations of the patent are encompassed by the more generic present application limitations, such as those in Norcott et al. directed to multiple ion implantation steps, whose initial step is this oxygen ions & produces buried defects, which are considered to encompass voids, and a second ion implantation produces an amorphous layer and may employ ions such as oxygen, or germanium, or bismuth, etc. Norcott et al.'s initially more generic oxidizing step is further defined in their dependent claims to affect annealing with parameters and gases as claimed. See above discussions concerning uniformity, also applicable here.

14. Claims 1-3, 7-8, 10, 12-15, 18, 21-24, 27-28, 31-33 & 35-38 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Hodge et al. (5,387,541).

Hodge et al. teach various possible routes for creating a porous layer within the silicon substrate, which may be oxidized so as to form a buried silicon layer. Specifically see the abstract; figures, noting figure 1 is a flow diagram suggesting various process routes, figure 2 illustrates blanket treatment, while figures 3 & 4 illustrate pattern treatments; col. 1 discusses known prior art porosity treatments, teaching that dopant level determines number & size of pores (col. 1, lines 8-17), with discussion of porosity levels, such as less than 50% (col. 1, lines 37); paragraph bridging cols. 1-2 discusses the importance of eliminating nonuniformity; col. 2, lines 14-29 sets forth the basic process sequence of manufacturing a porous silicon layer in the silicon wafer, then ion implanting into the porous layer causing amorphization therein, followed by recrystallization/annealing; col. 2 lines 36-68 & col. 5, lines 30-48 discussed electrolytic anodization using hydrofluoric acid (HF), with an exemplary current density of 5.5 mA/cm^2; col. 3, lines 1-3 teaching "pre-anodization p+ implant of the non-porous silicon surface and annealed in order to enhance uniformity of current flow through the wafer during anodization", which is considered to read on ion implanting a dopant, activation thereof by annealing, plus inherently creating a gradient effect in the porosity since ion doping will create a gradient concentration of dopant; col. 3, lines 4-53 & col.5, lines 49-col. 6, lines 3 ion implantation after annealing may include ions, such as Ge^+, Si^+, Sn^+, etc., where amorphous layer is produced & multiple ion implantations may be employed, with lines 44-54 noting optional use of masking to create amorphous silicon islands on porous silicon surface; col. 3, lines 58-64 & col. 6, lines 4-17 discussing typical annealing procedures, including preferred alternatives of 3 minutes rapid thermal annealing at 950°C in Ar and also 24 hours at 525°C in nitrogen or argon; col. 3, lines 65-col. 4, line 53 & col. 6, lines 56-col. 7, line 20 for various oxidizing procedures that may be employed when SOI material is desired to be produced, including possible patterning (col. 4, lines 10-19), a stabilizing oxidation process annealing at 300°C for an hour in flowing oxygen (col. 4, lines 20-31), a wet oxidation process that uses various sequences or temperatures, including wet oxidation at 800°C for

two hours, followed by 1090°C wet oxidation four minutes, where wet oxidation may typically include gases of H_2 & O_2 (col. 4, lines 32-54).

Hodge et al. does not explicitly state that the buried oxide layer, which they may produce, is "uniform" nor provide a degree of uniform as in applicants' specification definition, however as the same process steps as claimed are employ, the resultant effect would have been expected to be of analogous uniformity, whether one considers that term as a relative term, or within the scope of applicants' 20% thickness uniformity, as combined with defined upper & lower layers which are consistent with the results of Hodge et al., especially considering their teachings on enhancing uniformity of current flow during anodization, which would have been expected to enhance uniformity of porous layer formation, thus uniformity of resultant buried layer formed therefrom. Alternately, it would've been obvious to one of ordinary skill the art to employ the taught process for making SOI structures so as to make sufficiently uniform, reproducible layers useful for semiconductor device formation. Also see above analogous discussions.

14. Claims 4-6, 9, 11, 19-20, (25) 26 & 34 rejected under 35 U.S.C. 103(a) as being unpatentable over Hodge et al., optionally considering Ogata et al. (discussed above) for claims 4-6.

These dependent claims differ by requiring specific dopants, such as B, instead of generic teachings of the patent & specific parameters for the implantation, by claiming alternative variations on the activation/annealing process after implantation, including it art gas used in the oxygen ambient for oxidizing, specifically claiming repeating the process to create multilayered results, and claiming specific ion implantation parameters for the choice of Si ion as the "neutral ion", however these are all obvious variations relevant to routine experimentation & optimization of the process as taught by Hodge et al. and would not be considered to provide patentable significance to the process, as such routine experimentation considerations of the teachings of Hodge et al. would have been expected to encompass such parameters given their teachings that produce analogous results from otherwise like steps.

Alternately, with respect to claims 4-6 which are directed to specific dopants including the p-type dopant B, Hodge et al. suggest p-type ion implantation in general for the creation of the porous layer, where Ogata et al. provide the specific usefulness of boron for this purpose, thus substantiating the above asserted obviousness, as one of ordinary skill the art would have looked to analogous prior or such us about that at how to determine expected effective p-type dopants that may be on an implanted.

16. Claims 27-28 & 37 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-39, or 14-38 of U.S. Patent No. 6,486,037 (Norcott) or 6,800,518 (Bendernagel et al.), respectively, in view of Hodge et al.

Claims 27-28 & 37 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-25 of copending Application No. 10/674647 in view of Hodge et al. (discussed above in sections 14-15)

Although the conflicting claims are not identical, they are not patentably distinct from each other because while all of these patent or application claims have limitations involving oxidation processes, where ion implantation, or porous or void structures or the like are made, they are not directed to a "wet oxygen ambient" as part of the oxidation process, however Hodge et al., who teaches analogous processes, specifically teaches employing as part of their oxidation procedure a "wet oxidation" process, thus showing the expected effectiveness of such procedure with like materials to produce like SOI results, hence it would've been obvious to one of ordinary skill in the art to employ such oxidation parameters in oxidation steps of any of the Norcott or Bendernagel et al. patent is or the (467) application claims, especially as it is taught that such procedures are capable of changing eight "leaky" oxides such that it behaves substantially like a thermally grown oxide (col. 4, lines 32-53).

This is a provisional obviousness-type double patenting rejection for 10/674,647, because the conflicting claims have not in fact been patented.

17. Claims 1, 12-14 & 16-17 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Blewer et al. (5,023,200).

In Blewer et al., see the abstract; figures; col. 1, lines 65-col. 2, lines 10 (note teachings on uniformity of porous silicon layer, but no specific % values), 29-44 & 59-66; and col. 3, lines 30-col. 4, lines 32; col. 6, lines 13-68, especially 59-68 where the exemplary "about 10 mA for 100 mm wafer diameter" gives a value of 0.064 mA/cm^2; & claims especially 12-14. Blewer et al. specifically notes the known importance of uniformity in a buried oxide layer, however does not teach % values as defined in applicants' specification, however for this process with no critically different processing steps, like values will inherently have been encompassed. Also see above discussions on obviousness of producing uniformity.

18. References of Aspar et al. (6808967 B1), D'Arrigo et al. (6506658 B2) & Lin (7067387) contain analogous teachings to those discussed in above references, however are redundant for the claims as presently written. Sato et al. (5854123) is cited as of interest, as relating to analogous process employing electrolytic anodization for creating porosity, also discussing ion implantation & oxidation steps.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marianne L. Padgett whose telephone number is (571) 272-1425. The examiner can normally be reached on M-F from about 8:30 a.m. to 4:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Meeks, can be reached at (571) 272-1423. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available

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MLP/dictation software

5/30/2007-6/11/2007

/Marianne H. Padgett/

MARIANNE PADGETT
PRIMARY EXAMINER